National Semiconductor

PRELIMINARY

ECL Registered and Latched Programmable Array Logic (PAL®) Family

General Description

The registered and latched ECL PAL family consists of six device architectures, each offered in 10KH or 100K compatible versions. A maximum propagation delay of 6 ns (input to output) characterizes the performance of this ECL PAL series. The ECL PAL family utilizes National Semiconductor's advanced oxide-isolated process and proven Titanium Tungsten (Ti-W) fuse technology to provide user-programmable logic to replace conventional ECL SSI/MSI gates and flip-flops. Typical chip count reduction gained by using PAL devices is greater than 4:1.

This family allows the system engineer to customize the chip by opening fuse links to configure AND and OR gates to perform the desired logic function. Complex interconnections that previously required time-consuming layout are thus transferred from PC board to silicon where they can easily be modified during prototype checkout or production.

The PAL transfer function is the familiar sum-of-products implemented with a single array of fusible links. The PAL device incorporates a programmable AND array driving a fixed OR array. The AND term logic matrix incorporates 16 complementary inputs and 64 product terms. The 64 product terms are grouped into eight OR functions with eight product terms each. All devices in this family are provided with output polarity fuses. These fuses permit the designer to configure each output independently to produce either a logic high (by leaving the fuse intact) or a logic low (by programming the fuse) when the equation defining that output is satisfied. In addition, the ECL PAL family offers these options:

- Output registers
- Output latches
- Dual (split) clocks
- ORed (common) clocks

Product terms with all fuses programmed assume a logical high state, while product terms connected to both the true and complement of any input assume a logical low state. All product terms in an unprogrammed part are logically low. All input and I/O pins have on-chip 50 kΩ pull-down resistors. Registers consist of D-type flip-flops which are loaded in response to the low-to-high transition of the clock input(s). Latches are transparent while the enable inputs are low, and hold data while the enable inputs are high. Fuse symbols have been omitted from the logic diagrams to allow the designer use of the diagrams for logic editing.

These ECL PAL devices may be programmed on several TTL PLD programmers. Programming is accomplished with TTL voltage levels. Once the PAL is programmed and verified, an additional security fuse may be programmed to defeat verification. This feature gives the user a proprietary circuit which is difficult to copy.

Features

- High speed:
  - Combinatorial and latched outputs
    - **tpd = 6 ns max**
  - Registered outputs
    - t_{su} = 5 ns min
    - t_{clk} = 3.5 ns max
    - f_{max} = 117 MHz max
- Both 10 KH and 100K I/O compatible versions
- Eight output functions with feedback; eight dedicated inputs
- Eight registered or latched outputs, or four registered or latched outputs with four combinatorial outputs
- Individually programmable polarity on all logic outputs
- Output enable gate on all registered or latched outputs
- Reliable Titanium Tungsten fuses
- Security fuse to prevent direct copying
- Programmed on conventional TTL PLD programmers
- Fully Supported by PLAN™ Software
- Packaging:
  - 24-pin thin DIP (0.300")
  - 24-pin QUAD CERPAK

Applications

- Programmable replacement for ECL logic
- Programmable state machine
- Address or instruction decoding

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Temperature Under Bias (Ambient)	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
V_{EE} Relative to V_{CC}	−7V to +0.5V
Input Voltage	V_{EE} to +0.5V
Output Current	−50 mA
Lead Temperature (Soldering, 10 seconds)	300°C
ESD Tolerance	1000V
C_{ZAP} = 100 pF	
R_{ZAP} = 1500Ω	
Test Method: Human Body Model	
Test Specification: NSC SOP-5-028	

Electrical Characteristics Over Recommended Operating Conditions (Note 1)

Symbol	Parameter	Conditions		T_A	Min	Max	Units
V_{IH}	High Level Input Voltage	Guaranteed Input Voltage High For All Inputs	10 KH	0°C +25°C +75°C	−1170 −1130 −1070	−840 −810 −735	mV
			100K	0°C to +85°C	−1165	−880	
V_{IL}	Low Level Input Voltage	Guaranteed Input Voltage Low For All Inputs	10 KH	0°C +25°C +75°C	−1950 −1950 −1950	−1480 −1480 −1450	mV
			100K	0°C to +85°C	−1810	−1475	
V_{OH}	High Level Output Voltage	V_{IN} = V_{IH} Max. or V_{IL} Min.	10 KH	0°C +25°C +75°C	−1020 −980 −920	−840 −810 −735	mV
			100K	0°C to +85°C	−1025	−880	
V_{OL}	Low Level Output Voltage	V_{IN} = V_{IH} Max. or V_{IL} Min.	10 KH	0°C +25°C +75°C	−1950 −1950 −1950	−1630 −1630 −1600	mV
			100K	0°C to +85°C	−1810	−1620	
I_{IH}	High Level Input Current (Note 4)	V_{IN} = V_{IH} Max.	10 KH	0°C +75°C		220	μA
			100K	0°C to +85°C			
I_{IL}	Low Level Input Current	V_{IN} = V_{IL} Min. Except I/O Pins	10 KH	0°C +75°C	0.5		μA
			100K	0°C to +85°C			
I_{EE}	Supply Current	V_{EE} = Min. All Inputs and Outputs Open	LD8, LD4, RD4, RC4		−260		mA
			RD8, RC8		−280		

Recommended Operating Conditions

Symbol	Parameter		Min	Typ	Max	Units
V_{EE}	Supply Voltage	10 KH	−5.46	−5.2	−4.94	V
		100K	−4.73	−4.5	−4.27	
T	Operating Temperature (Note 2)	10 KH	0		+75	°C
		100K	0		+85	
R_L	Standard 10 KH/100K Load			50		Ω
C_L	Standard 10 KH/100K Load			5		pF
t_{SU}	Setup Time of Input or Feedback (Note 3)		5			ns
t_H	Input Hold Time (Note 3)		0			ns
t_W	Clock or Enable Pulse Width (Note 3)		4			ns
t_{WMR}	Master Reset Pulse Width (Note 3)		4			ns

Note 1: This product family has been designed to meet the specification in the test table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained.

Note 2: Operating temperatures for circuits in Dual-In-Line packages are specified as ambient temperatures (T_A) with circuits mounted in socket or printed circuit board and transverse airflow exceeding 500 linear feet per minute. Operating temperatures for circuits packaged in QUAD CERPAK are specified as case temperatures (T_C).

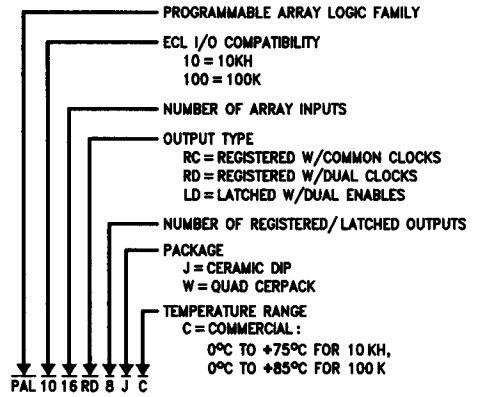
Note 3: Applies to registered and latched outputs.

Note 4: Except for clock inputs (350 μA) and MR (1 mA).

Ordering Information

The 12 products in the family are differentiated by their logic level compatibility (10 KH or 100K), by their output type (registered, latched or mixed combinatorial) and by their clock configuration (Common ORed or Dual clocks). The family consists of the following products:

Part Number	Description
PAL1016RC8 PAL10016RC8	8 Registered Outputs with Common ORed Clock
PAL1016RD8 PAL10016RD8	8 Registers with Dual Clocks (4 Registers Each)
PAL1016RC4 PAL10016RC4	4 Registers (Common Clock) Plus 4 Combinatorial I/Os
PAL1016RD4 PAL10016RD4	4 Registers (Dual Clocks) Plus 4 Combinatorial I/Os
PAL1016LD8 PAL10016LD8	8 Latches with Dual Clocks (4 Latches Each)
PAL1016LD4 PAL10016LD4	4 Latches (Dual Clocks) Plus 4 Combinatorial I/Os



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Switching Characteristics Over Recommended Operating Conditions

Output Load: $R_L = 50\Omega$ to $-2.0V$, $C_L = 5$ pF to GND

Symbol	Parameter	Measured		Min	Max	Units
		From	To			
t_{CLK} (Note 1)	Clock to Output or Feedback	$C_n \uparrow$	Q		3.5	ns
t_{LE} (Note 2)	Enable to Output or Feedback	$\overline{L_n} \downarrow$	Q		3.5	ns
t_{PD} (Note 2, 3)	Input or Feedback to Output	I	Q or I/O		6	ns
t_{PLH} (Note 1, 2)	Output Enable	$\overline{G} \downarrow$	Q $\uparrow$		4.0	ns
t_{PHL} (Note 1, 2)	Output Disable	$\overline{G} \uparrow$	Q $\downarrow$		4.0	ns
t_{MR} (Note 1, 2)	Master Reset to Output	MR $\uparrow$	Q $\downarrow$		5.5	ns
f_{MAX} (Note 1, 4)	Maximum Frequency				117	MHz
t_r	Output Rise Time	Measured Between 20% and 80% points		0.5	2.5	ns
t_f	Output Fall Time			0.5	2.5	ns

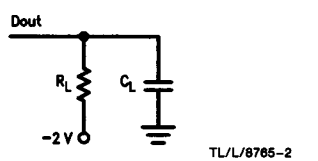
Note 1: Applies to registered outputs.

Note 2: Applies to latched outputs.

Note 3: Applies to combinatorial outputs.

Note 4: $f_{MAX} = (t_{SU} + t_{CLK})^{-1}$

Test Load



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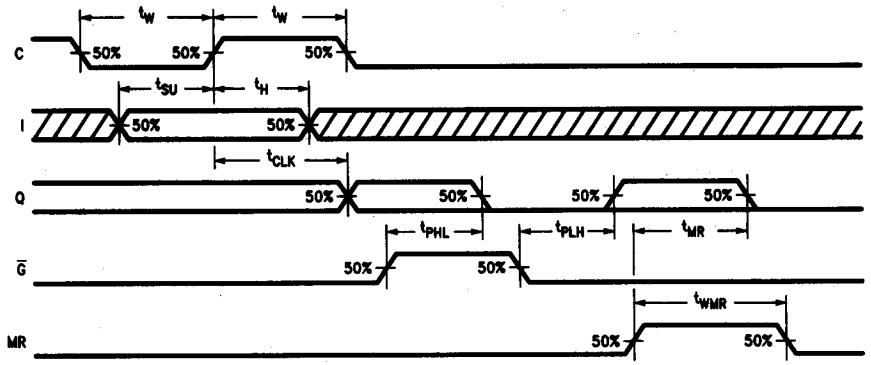
Timing Waveform—All Registered Outputs



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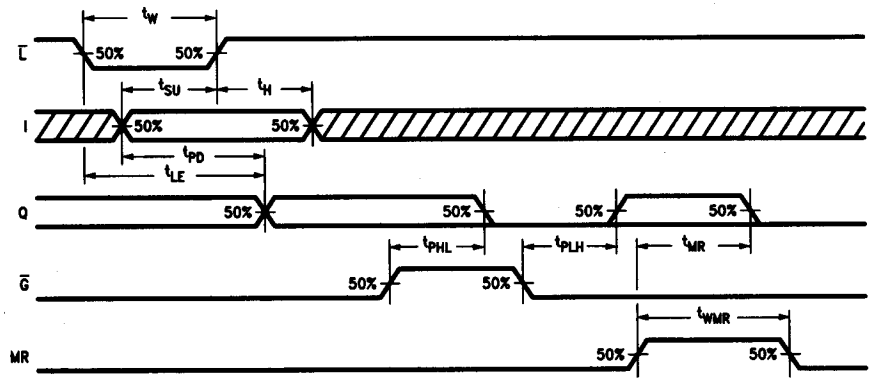
Timing Waveform—All Latched Outputs



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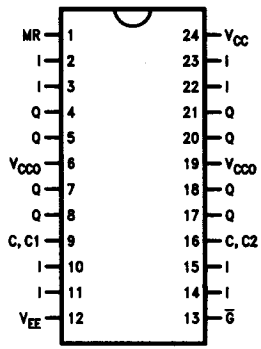
Connection Diagrams (24-pin Dual-In-Line Packages)

PAL1016RC8/PAL10016RC8
PAL1016RD8/PAL10016RD8



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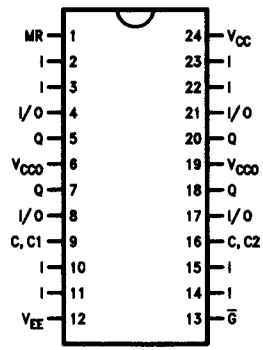
PAL1016RC4/PAL10016RC4
PAL1016RD4/PAL10016RD4



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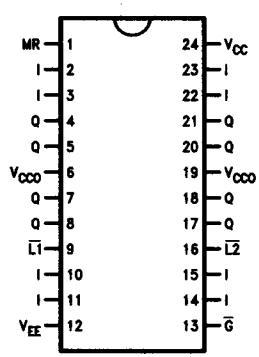
PAL1016LD8/PAL10016LD8



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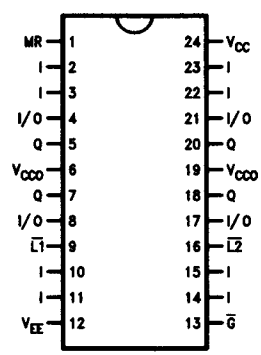
PAL1016LD4/PAL10016LD4



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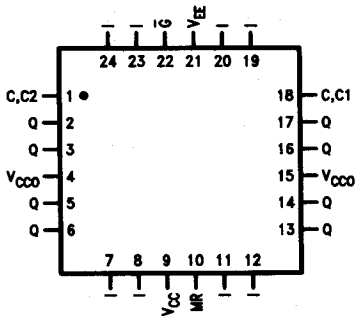
Pin Descriptions

Pin	Description
I	Eight dedicated inputs to logic array.
Q	Four or eight outputs from registered or latched logic functions.
I/O	Four outputs from combinatorial logic functions on 'RC4, 'RD4 and 'LD4. Pin signal fed back as input into logic array. Pin can be used as input or output.
C, C1	Clock input for registers on output pins* 4, 5, 7 and 8 on dual-clock devices; ORed with C2 to control all registers on common-clock devices. Data is written into registers on rising edge of clock.
C, C2	Clock input for registers on output pins* 17, 18, 20 and 21 on dual-clock devices; ORed with C1 to control all registers on common-clock devices. Data is written into registers on rising edge of clock.
$\overline{L1}$	Latch enable input for latches on output pins* 4, 5, 7 and 8. Latches are transparent (data written into latch) while the enable signal is low.
$\overline{L2}$	Latch enable input for latches on output pins* 17, 18, 20 and 21. Latches are transparent (data written into latch) while the enable signal is low.
MR	Master Reset input. Asynchronously resets all registers or latches to the low state while MR is high (overrides clock and latch enable).
$\overline{G}$	Output enable input. Enables output drivers while $\overline{G}$ is low; forces all registered or latched output drivers to the low state as long as $\overline{G}$ is high. Register or latch contents and feedbacks are not affected. Combinatorial outputs are not affected.
V_{EE}	Supply voltage.
V_{CC}	Ground for internal circuitry.
V_{CCO}	Ground for output drivers (4 outputs per V_{CCO}).

*Corresponds to DIP pinout

Connection Diagrams (24-pin Quad Cerpak)

PAL1016RC8/PAL10016RC8
PAL1016RD8/PAL10016RD8



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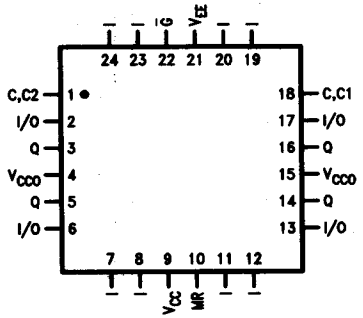
PAL1016RC4/PAL10016RC4
PAL1016RD4/PAL10016RD4



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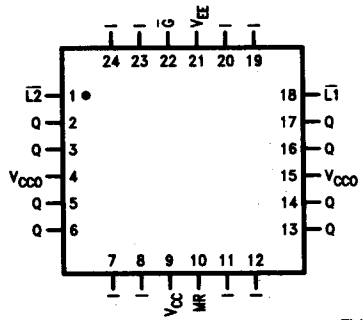
PAL1016LD8/PAL10016LD8



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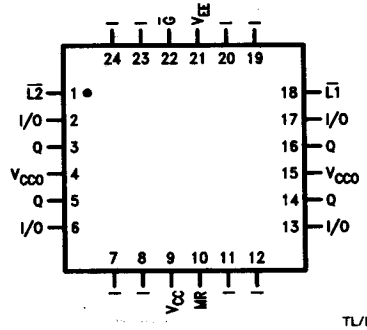
PAL1016LD4/PAL10016LD4



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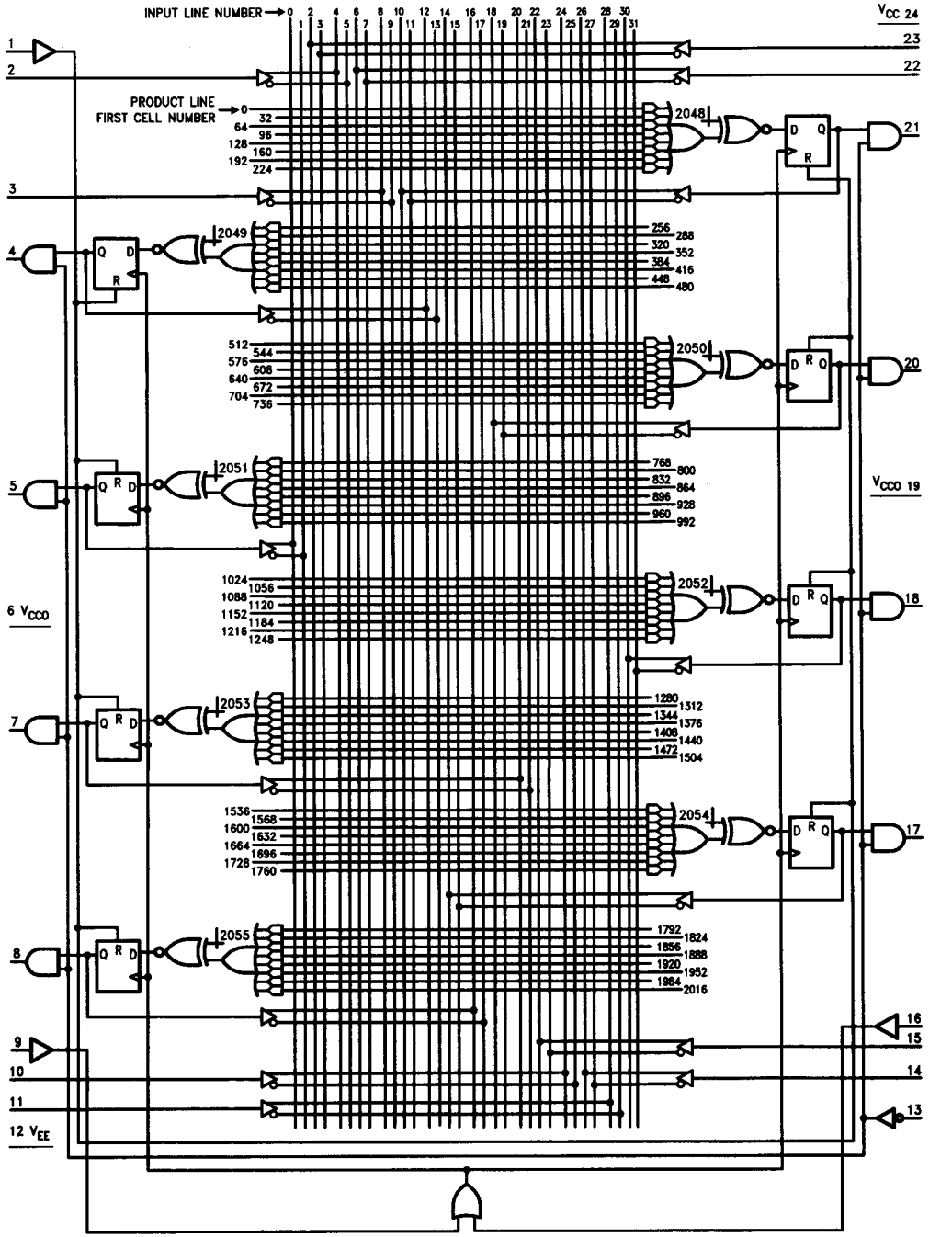
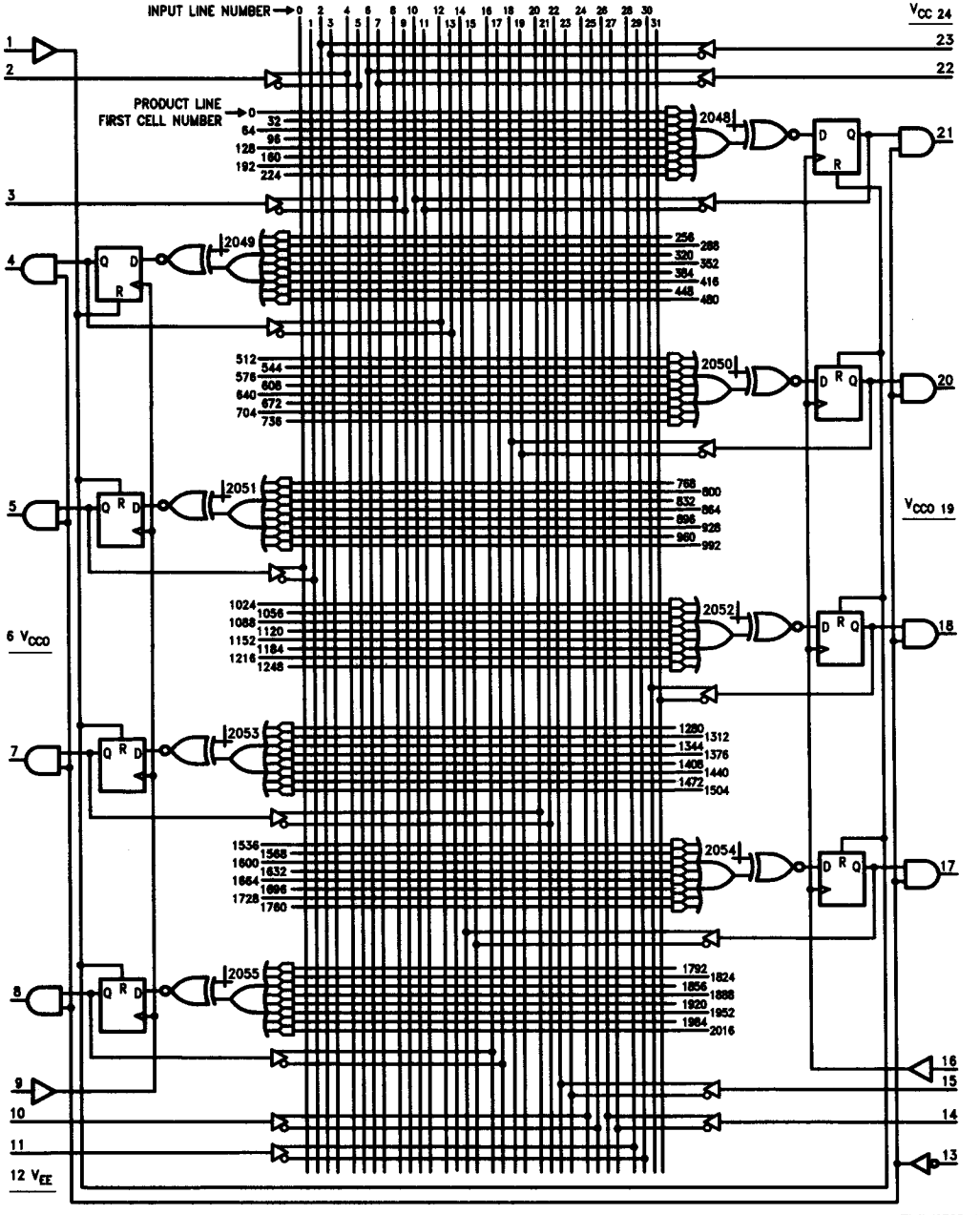
Logic Diagram PAL1016RC8/PAL10016RC8



JEDEC logic array cell number = product line first cell number + input line number.

Logic Diagram PAL1016RD8/PAL10016RD8



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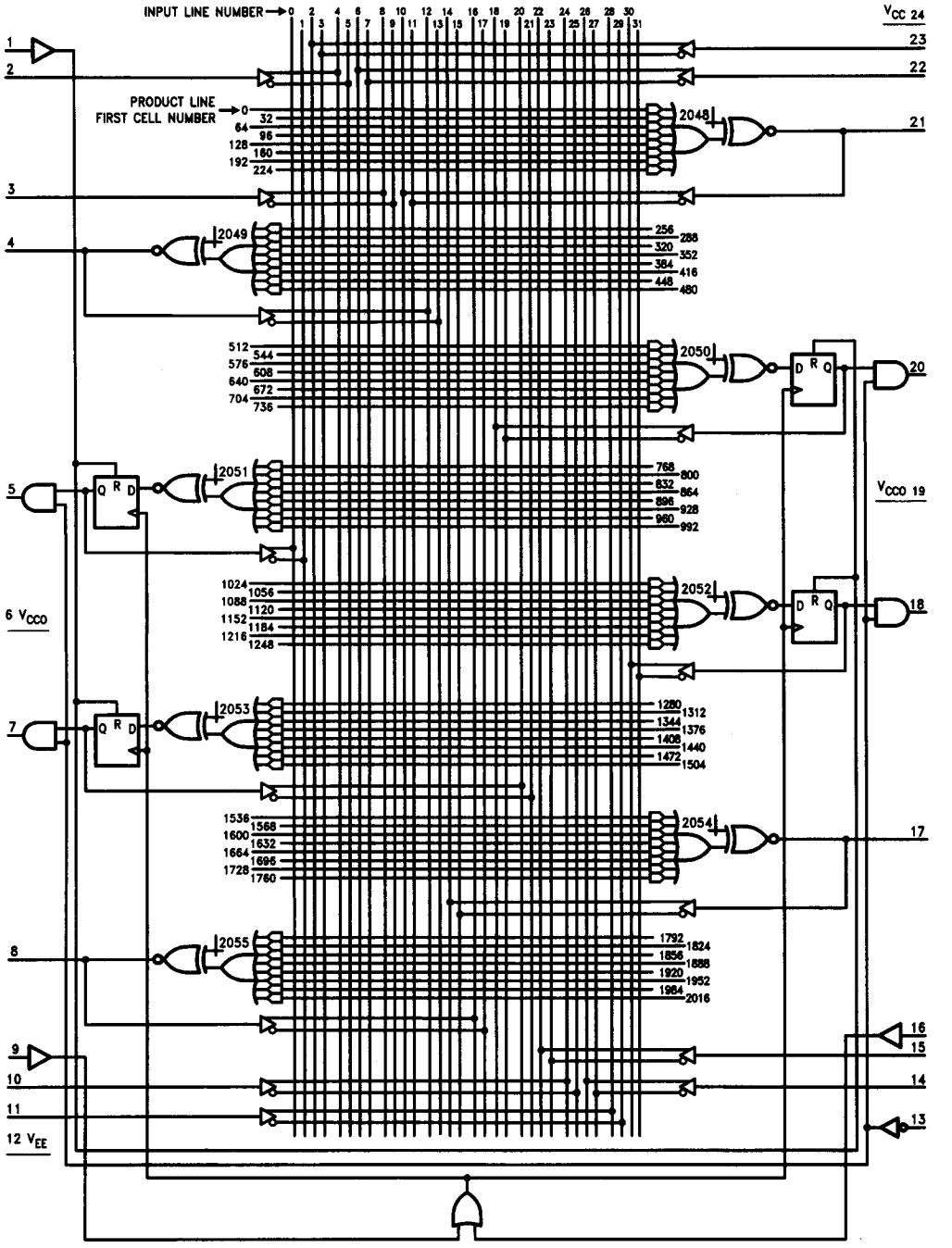
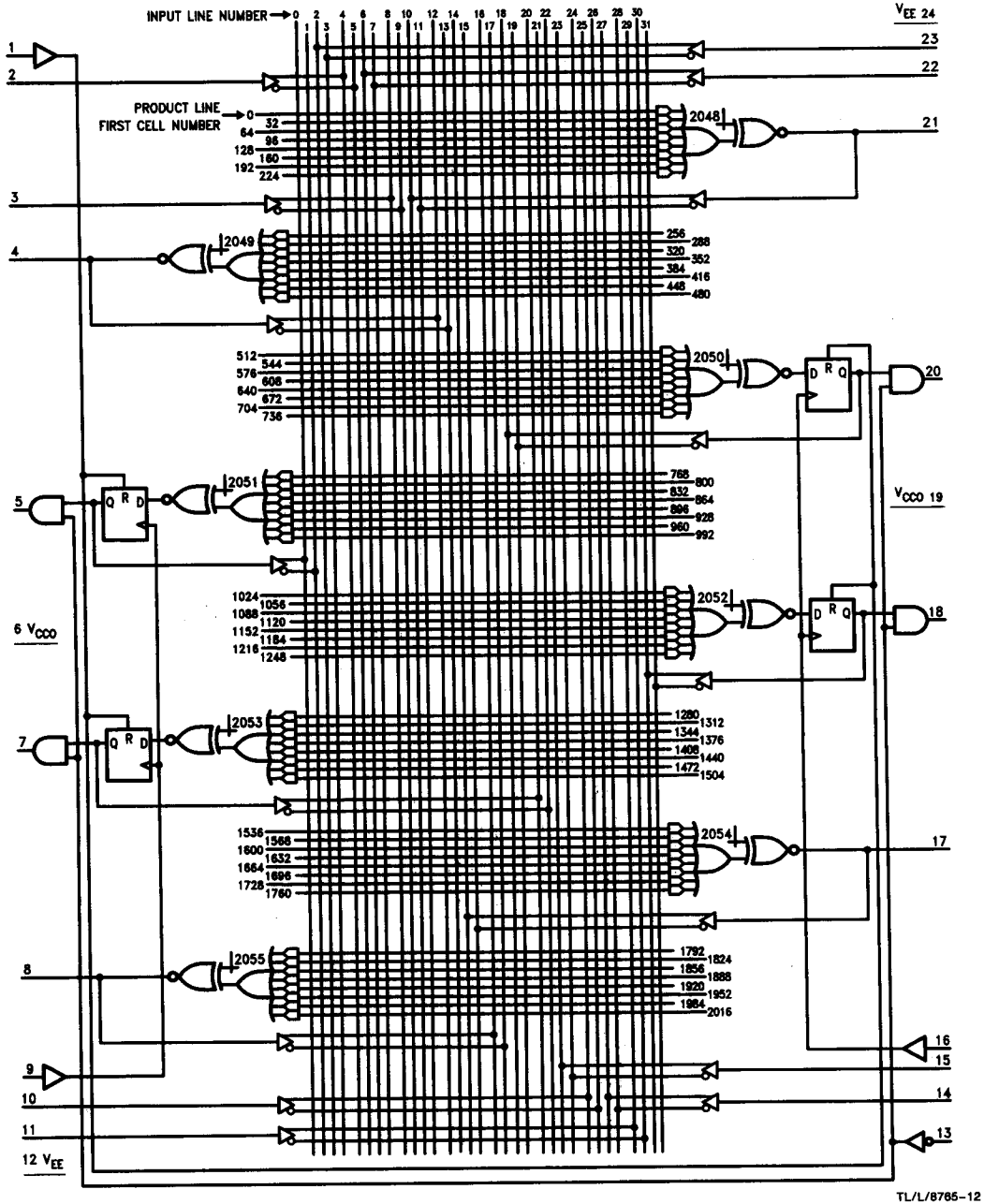
JEDEC logic array cell number = product line first cell number + input line number.

Logic Diagram PAL1016RC4/PAL10016RC4



JEDEC logic array cell number = product line first cell number + input line number.

Logic Diagram PAL1016RD4/PAL10016RD4



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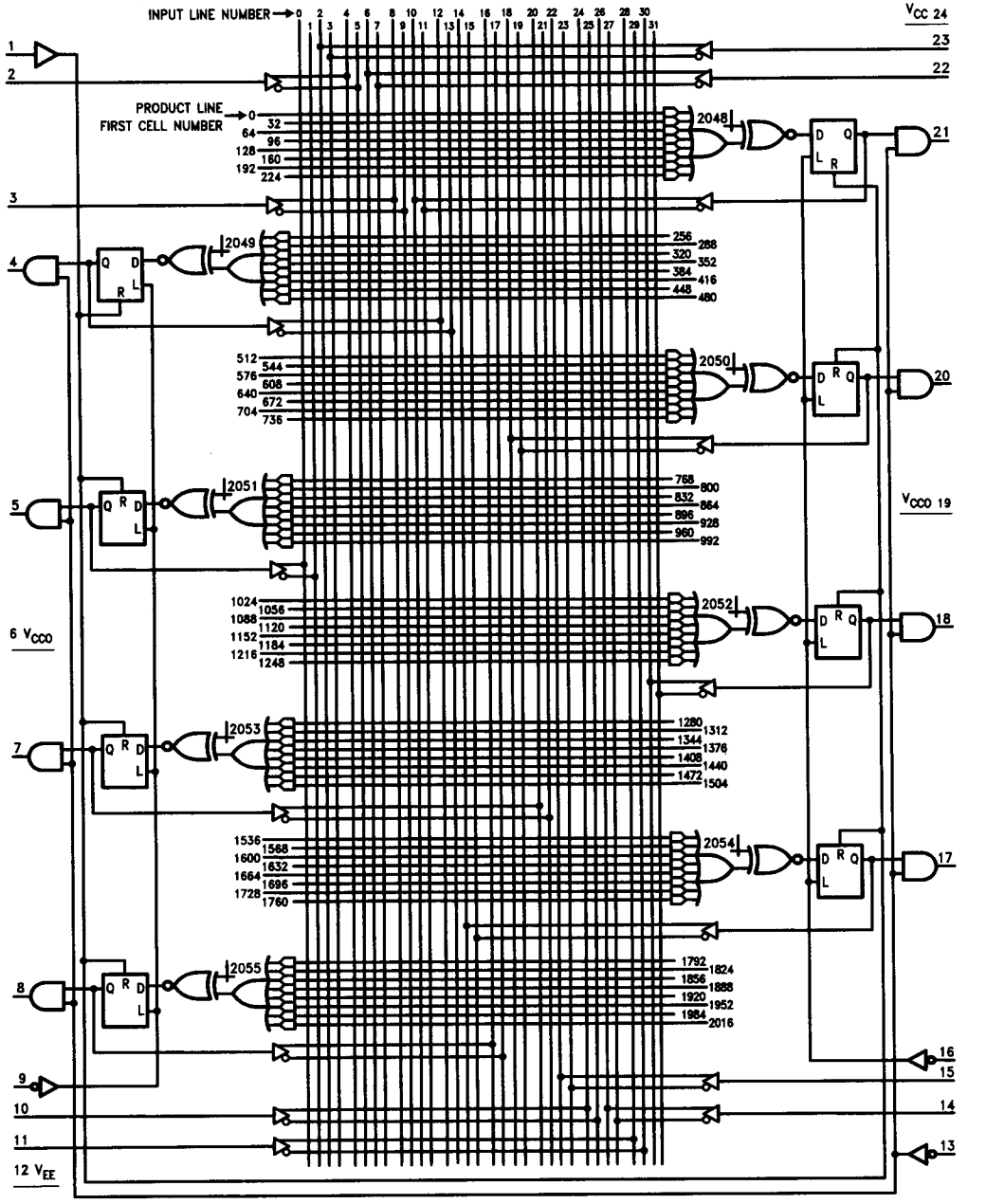
JEDEC logic array cell number = product line first cell number + input line number.

Logic Diagram PAL1016LD8/PAL10016LD8



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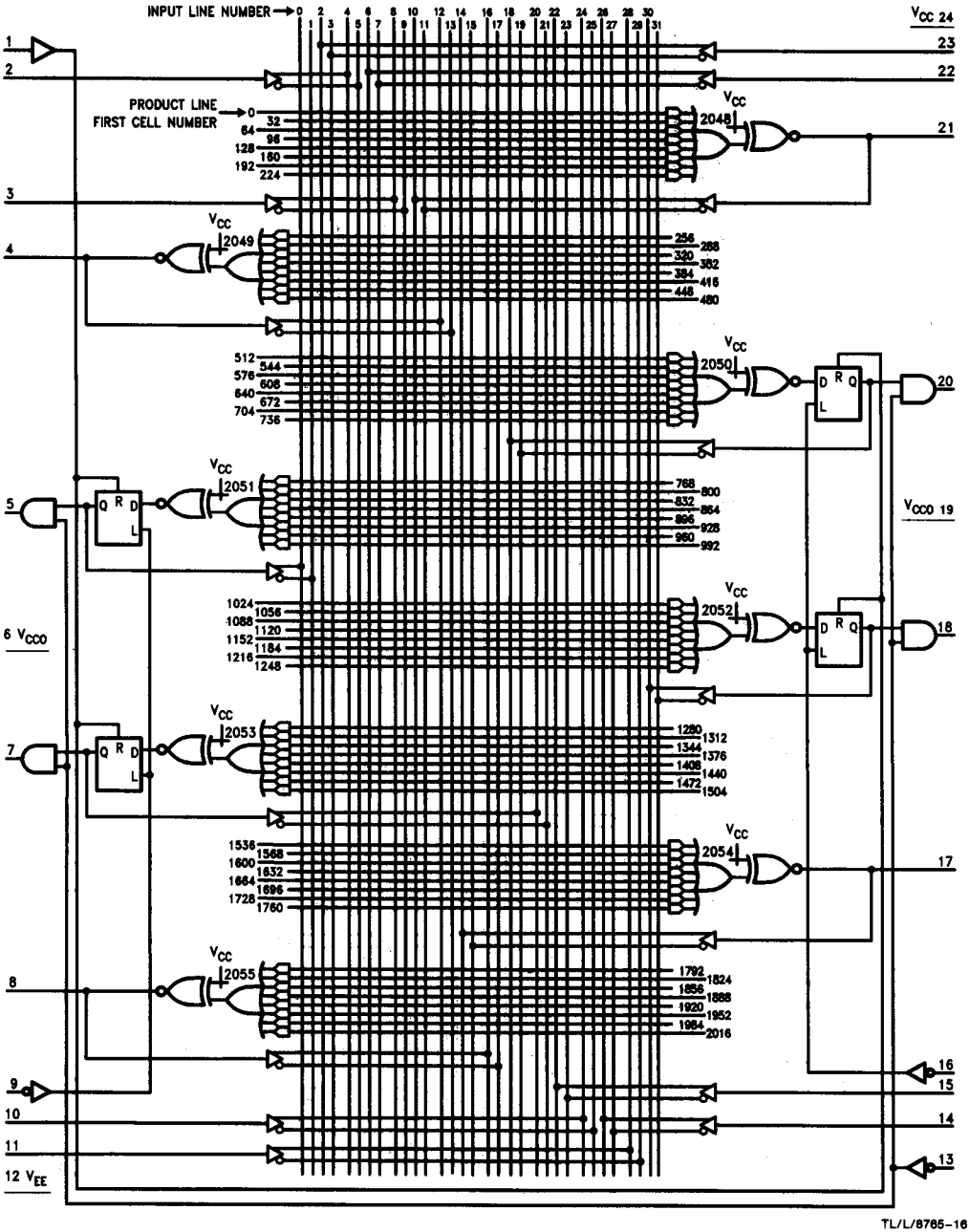
JEDEC logic array cell number = product line first cell number + input line number.

Logic Diagram PAL1016LD4/PAL10016LD4



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JEDEC logic array cell number = product line first cell number + input cell number.

Functional Testing

As with all field-programmable devices, the user of ECL PAL devices provides the final manufacturing step. While National's PAL devices undergo extensive testing when they are manufactured, their logic function can be fully tested only after they have been programmed to the user's pattern.

To ensure that the programmed PAL devices will operate properly in your system, National Semiconductor (along with most other manufacturers of PAL devices) strongly recommends that PAL devices be functionally tested before they are installed in your system. Even though the number of post-programming functional failures is small, testing the logic function of the PAL devices before they reach system assembly will save board debugging and rework costs. Refer to National Semiconductor's Application Note #351 and the *Programmable Logic Design Guide* for more information about the functional testing of PAL devices.

For a list of current programming support tools for ECL PAL devices, please contact your local National Semiconductor sales office.